

CLAIMS

What is claimed is:

1. A semiconductor junction device, comprising:
a substrate;
a first material extending substantially vertically from said substrate;
said first material having a sidewall and an upper surface; and
a second material;
said second material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first material;
wherein a junction is formed between said first and second materials.
2. A semiconductor junction device as recited in claim 1, further comprising:
a first electrical contact connected to said first material; and
a second electrical contact connected to said second material.
3. A semiconductor junction device as recited in claim 1, wherein said junction comprises a *pn* junction.
4. A semiconductor junction device as recited in claim 1, wherein said junction comprises an *in* junction.
5. A semiconductor junction device as recited in claim 1, wherein said junction comprises a *pi* junction.
6. A semiconductor junction device, comprising:
a substrate;
a first material extending substantially vertically from said substrate;
said first material comprising a semiconductor material;
said first material having a sidewall and an upper surface; and

a second material;
said second material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first material;
wherein a junction is formed between said first and second materials.

7. A semiconductor junction device as recited in claim 6, further comprising:

a first electrical contact connected to said first material; and
a second electrical contact connected to said second material.

8. A semiconductor junction device as recited in claim 6, wherein said junction comprises a *pn* junction.

9. A semiconductor junction device as recited in claim 6, wherein said junction comprises an *in* junction.

10. A semiconductor junction device as recited in claim 6, wherein said junction comprises a *pi* junction.

11. A semiconductor junction device, comprising:
a substrate;
a first material extending substantially vertically from said substrate;
said first material having a sidewall and an upper surface; and
a second material;
said second material comprising a semiconductor material;
said second material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first material;
wherein a junction is formed between said first and second materials.

12. A semiconductor junction device as recited in claim 11, further comprising:

a first electrical contact connected to said first material; and
a second electrical contact connected to said second material.

13. A semiconductor junction device as recited in claim 11, wherein said junction comprises a *pn* junction.

14. A semiconductor junction device as recited in claim 11, wherein said junction comprises an *in* junction.

15. A semiconductor junction device as recited in claim 11, wherein said junction comprises a *pi* junction.

16. A semiconductor junction device, comprising:
a substrate;
a first semiconductor material extending substantially vertically from said substrate;
said first material having a sidewall and an upper surface; and
a second semiconductor material;
said second material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first material;
wherein a junction is formed between said first and second materials.

17. A semiconductor junction device as recited in claim 16, further comprising:

a first electrical contact connected to said first material; and
a second electrical contact connected to said second material.

18. A semiconductor junction device as recited in claim 16, wherein said junction comprises a *pn* junction.

19. A semiconductor junction device as recited in claim 16, wherein said junction comprises an *in* junction.

20. A semiconductor junction device as recited in claim 16, wherein said junction comprises a *pi* junction.

21. A semiconductor junction device, comprising:
a substrate;
a first material extending substantially vertically from said substrate;
said first material comprising a doped semiconductor material;
said first material having a sidewall and an upper surface; and
a second material;
said second material comprising a semiconductor material;
said second material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first material;
wherein a junction is formed between said first and second materials.

22. A semiconductor junction device as recited in claim 21, further comprising:
a first electrical contact connected to said first material; and
a second electrical contact connected to said second material.

23. A semiconductor junction device as recited in claim 21, wherein said junction comprises a *pn* junction.

24. A semiconductor junction device as recited in claim 21, wherein said junction comprises an *in* junction.

25. A semiconductor junction device as recited in claim 21, wherein said junction comprises a *pi* junction.

26. A semiconductor junction device, comprising:
a substrate;
a first material extending substantially vertically from said substrate;
said first material comprising a semiconductor material;
said first material having a sidewall and an upper surface; and
a second material;
said second material comprising a doped semiconductor material;
said second material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first material;
wherein a junction is formed between said first and second materials.

27. A semiconductor junction device as recited in claim 26, further comprising:
a first electrical contact connected to said first material; and
a second electrical contact connected to said second material.

28. A semiconductor junction device as recited in claim 26, wherein said junction comprises a *pn* junction.

29. A semiconductor junction device as recited in claim 26, wherein said junction comprises an *in* junction.

30. A semiconductor junction device as recited in claim 26, wherein said junction comprises a *pi* junction.

31. A semiconductor junction device, comprising:
a substrate;
a first doped semiconductor material extending substantially vertically from said substrate;
said first material having a sidewall and an upper surface; and
a second doped semiconductor material;

said second material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first material;

wherein a junction is formed between said first and second materials.

32. A semiconductor junction device as recited in claim 31, further comprising:

a first electrical contact connected to said first material; and

a second electrical contact connected to said second material.

33. A semiconductor junction device as recited in claim 31, wherein said junction comprises a *pn* junction.

34. A semiconductor junction device, comprising:

a substrate;

a first semiconductor material extending substantially vertically from said substrate;

said first material having a sidewall and an upper surface;

a second semiconductor material;

said second material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first semiconductor material; and

a third semiconductor material;

said third material joined to at least a portion of said second material;

wherein a first junction is formed between said first and second materials;

wherein a second junction is formed between said second and third materials;

and

wherein said first material is electrically isolated from said third material.

35. A semiconductor junction device as recited in claim 34, further comprising:

a first electrical contact connected to said first material;

a second electrical contact connected to said second material; and

a third electrical contact connected to said third material.

36. A semiconductor junction device as recited in claim 34, wherein said first junction comprises a *pn* junction.

37. A semiconductor junction device as recited in claim 34, wherein said first junction comprises an *in* junction.

38. A semiconductor junction device as recited in claim 34, wherein said first junction comprises a *pi* junction.

39. A semiconductor junction device as recited in claim 34, wherein said second junction comprises a *pn* junction.

40. A semiconductor junction device as recited in claim 34, wherein said second junction comprises an *in* junction.

41. A semiconductor junction device as recited in claim 34, wherein said second junction comprises a *pi* junction.

42. A semiconductor junction device as recited in claim 34, wherein said first and second junctions are configured as a bipolar transistor.

43. A semiconductor junction device as recited in claim 42, wherein said bipolar transistor comprises a *npn* transistor.

44. A semiconductor junction device as recited in claim 42, wherein said bipolar transistor comprises a *pnp* transistor.

45. A semiconductor junction device as recited in claim 34, wherein said first and second junctions are configured as a *pin* junction device.

46. A semiconductor junction device as recited in claim 34, wherein said first and second junctions are configured as a *pip* junction device.

47. A semiconductor junction device, comprising:
a substrate;
a first material extending substantially vertically from said substrate;
said first material comprising a doped semiconductor material;
said first material having a sidewall and an upper surface;
a second material;
said second material comprising a semiconductor material;
said second material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first material; and
a third material;
said third material comprising a doped semiconductor material;
said third material joined to at least a portion of said second material;
wherein a first junction is formed between said first and second materials;
wherein a second junction is formed between said second and third materials;
and
wherein said first material is electrically isolated from said third material.

48. A semiconductor junction device as recited in claim 47, further comprising:

a first electrical contact connected to said first material;
a second electrical contact connected to said second material; and
a third electrical contact connected to said third material.

49. A semiconductor junction device as recited in claim 47, wherein said first junction comprises a *pn* junction.

50. A semiconductor junction device as recited in claim 47, wherein said first junction comprises an *in* junction.

51. A semiconductor junction device as recited in claim 47, wherein said first junction comprises a *pi* junction.

52. A semiconductor junction device as recited in claim 47, wherein said second junction comprises a *pn* junction.

53. A semiconductor junction device as recited in claim 47, wherein said second junction comprises an *in* junction.

54. A semiconductor junction device as recited in claim 47, wherein said second junction comprises a *pi* junction.

55. A semiconductor junction device as recited in claim 47, wherein said first and second junctions are configured as a bipolar transistor.

56. A semiconductor junction device as recited in claim 55, wherein said bipolar transistor comprises a *npn* transistor.

57. A semiconductor junction device as recited in claim 55, wherein said bipolar transistor comprises a *pnp* transistor.

58. A semiconductor junction device as recited in claim 47, wherein said first and second junctions are configured as a *pin* junction device.

59. A semiconductor junction device as recited in claim 47, wherein said first and second junctions are configured as a *pip* junction device.

60. A semiconductor junction device, comprising:
a substrate;
a first doped semiconductor material extending substantially vertically from said substrate;
said first doped semiconductor material having a sidewall and an upper surface;
a second doped semiconductor material;
said second doped semiconductor material joined to at least a portion of said sidewall and to at least a portion of said upper surface of said first doped semiconductor material; and
a third doped semiconductor material;
said third doped semiconductor material joined to at least a portion of said second doped semiconductor material;
wherein a first junction is formed between said first and second materials;
wherein a second junction is formed between said second and third materials;
and
wherein said first material is electrically isolated from said third material.

61. A semiconductor junction device as recited in claim 60, further comprising:
a first electrical contact connected to said first material;
a second electrical contact connected to said second material; and
a third electrical contact connected to said third material.

62. A semiconductor junction device as recited in claim 60, wherein said first junction comprises a *pn* junction.

63. A semiconductor junction device as recited in claim 60, wherein said second junction comprises a *pn* junction.

64. A semiconductor junction device as recited in claim 60, wherein said first and second junctions are configured as a bipolar transistor.

65. A semiconductor junction device as recited in claim 64, wherein said bipolar transistor comprises a *npn* transistor.

66. A semiconductor junction device as recited in claim 64, wherein said bipolar transistor comprises a *pnp* transistor.

67. A method of fabricating a semiconductor junction device, comprising:
forming a region of a first material extending substantially vertically from a substrate;
said first material having a sidewall and an upper surface; and
depositing a second material on at least a portion of said sidewall and on at least a portion of said upper surface of said first material;
wherein a junction is formed between said first and second materials.

68. A method as recited in claim 67, wherein said junction comprises a *pn* junction.

69. A method as recited in claim 67, wherein said junction comprises an *in* junction.

70. A method as recited in claim 67, wherein said junction comprises a *pi* junction.

71. A method as recited in claim 67, wherein at least one of said materials comprises a semiconductor material.

72. A method as recited in claim 67, wherein both of said materials comprise semiconductor materials.

73. A method as recited in claim 67, wherein at least one of said materials comprises a doped semiconductor material.

74. A method as recited in claim 67, wherein both of said materials comprises a doped semiconductor material.

75. A method of fabricating a semiconductor junction device, comprising:
forming a region of a first semiconductor material extending substantially vertically from a substrate;
said first material having a sidewall and an upper surface;
depositing a second semiconductor material on at least a portion of said sidewall and on at least a portion of said upper surface of said first material;
wherein a first junction is formed between said first and second materials;
forming a region of a third semiconductor material joined to at least a portion of said second material;
wherein a second junction is formed between said second and third materials;
and
wherein said first material is electrically isolated from said third material.

76. A method as recited in claim 75, wherein said first junction comprises a *pn* junction.

77. A method as recited in claim 75, wherein said first junction comprises an *in* junction.

78. A method as recited in claim 75, wherein said first junction comprises a *pi* junction.

79. A method as recited in claim 75, wherein said second junction comprises a *pn* junction.

80. A method as recited in claim 75, wherein said second junction comprises an *in* junction.

81. A method as recited in claim 75, wherein said second junction comprises a *pi* junction.

82. A method as recited in claim 75, wherein said first and second junctions are configured as a bipolar transistor.

83. A method as recited in claim 82, wherein said bipolar transistor comprises a *npn* transistor.

84. A method as recited in claim 82, wherein said bipolar transistor comprises a *pn*p transistor.

85. A method as recited in claim 75, wherein said first and second junctions are configured as a *pin* junction device.

86. A method as recited in claim 75, wherein said first and second junctions are configured as a *pip* junction device.

87. A method as recited in claim 75, wherein at least one of said materials comprises a doped semiconductor material.

88. A method as recited in claim 75, where at least two of said materials comprising doped semiconductor materials.

89. A method as recited in claim 75, wherein said first, second and third materials comprise doped semiconductor materials.

90. A method of fabricating a semiconductor junction device, comprising:
forming a region of a first material extending substantially vertically from a substrate;
processing a collector *n*-doped region on a *p*-type silicon substrate by high-energy phosphorus ion implantation;
forming an oxide buffer layer over the surface of the substrate by thermal oxidation;
annealing the substrate at high temperature so that the phosphorus atoms are redistributed;
depositing a silicon nitride layer over the oxide layer to form *n*-hill cap layer;
depositing photoresist over the silicon nitride layer;
patterning said photoresist using a first lithography mask;
selectively removing the nitride-oxide double layer and anisotropically etching the *n*-doped silicon to reach the *p*-substrate and an *n*-hill having a least one sidewall and an upper surface is formed;
implanting boron ions to increase *p*-type doping in the field around the *n*-hill;
depositing silicon oxide over said *p*-substrate and said *n*-hill;
chemically-mechanically planarizing said silicon-dioxide;
etching back said silicon dioxide to form isolation regions around said *n*-hill;
depositing and patterning photoresist using a second lithography mask to define intrinsic and extrinsic base regions on said *n*-hill;
forming a *p*-region on one side of the *n*-hill by ion implanting the intrinsic base region; and
extending the *p*-region over the surface of the *n*-hill by ion implanting the extrinsic base region.

91. A method as recited in claim 90, further comprising:
removing the photoresist;
forming a doped polysilicon layer over said *n*-hill and substrate;
depositing undoped polysilicon over said doped polysilicon layer;
chemically-mechanically planarizing the polysilicon layers;

etching back said polysilicon layers selectively to the formed base so that at least a portion of the active sidewall is in contact with the polysilicon;

using a third lithography mask, removing polysilicon from the front and back sides of the n -hill to define emitter and collector active regions;

etching away the nitride layer and depositing passivation oxide;

carrying out annealing and emitter drive-in diffusion; and

forming electrical contacts to said base, emitter and collector regions.